EDITED BY BILL TRAVIS & ANNE WATSON SWAGER

Inexpensive relays form digital potentiometer

ROBERT PERRIN, Z-WORLD, DAVIS, CA

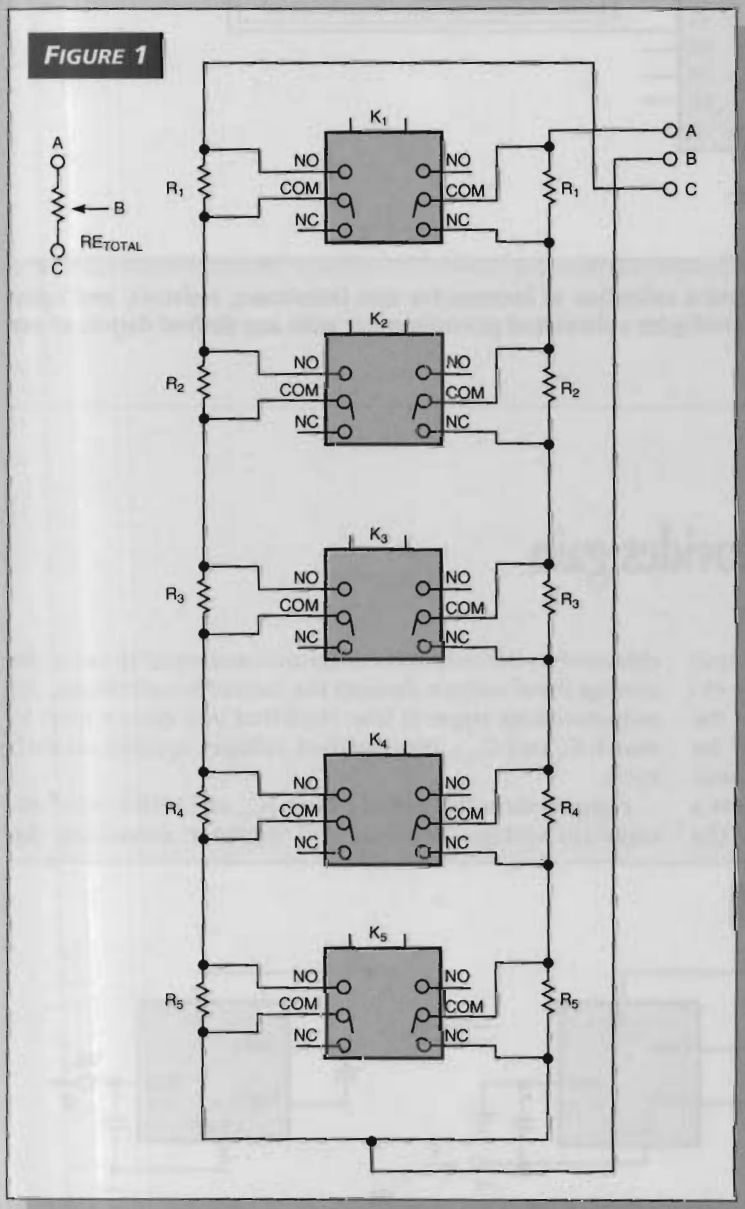
A project posed the challenge of replacing existing analog potentiometers (used to set brightness and contrast levels) in video monitors with digitally controlled potentiometers. The different brands and models of monitors presented widely varying voltages across the potentiometers. The design had to

- accept digital controls,
- be purely resistive,
- tolerate 60V dc or ac between any two points,
- be able to dissipate 1W,
- be scalable for future systems, and
- have high isolation between the digital controller and the simulated potentiometer.

Also, during switching, the wiper could not become open-circuited, and it had to be able to travel end-to-end.

Existing digitally controlled potentiometers were not up to the task. FET switches faced special challenges with the ac-voltage isolation criterion. The design in **Figure 1** uses inexpensive relays to build a digitally controlled potentiometer. The relays switch their respective resistors above or below the tap. With all the relays de-energized, the potentiometer has the

FIGURE 1

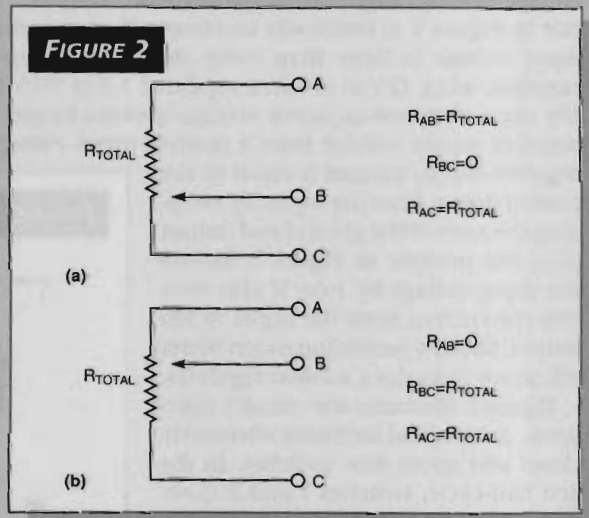


A handful of relays and fixed resistors replaces an analog potentiometer. The resolution of the simulated potentiometer is one part in 2^n, where n is the number of relays.

TABLE 1—RESISTOR VALUES FOR DIGITAL POTENTIOMETER

Reference designator	Resistance
R_1	$R_{TOTAL}/2^1$
R_2	$R_{TOTAL}/2^2$
R_3	$R_{TOTAL}/2^3$
R_4	$R_{TOTAL}/2^4$
R_5	$R_{TOTAL}/2^5$
R_n	$R_{TOTAL}/2^n$

FIGURE 2



De-energizing all the relays in Figure 1's circuit results in the configuration in a; energizing all the relays results in the configuration in b.

configuration shown in **Figure 2a**. With all the relays energized, the relay takes the form shown in **Figure 2b**. The resistors are weighted in a $R_{TOTAL}/2^n$ relationship. This weighting gives a good approximation of a linear taper with 32 (2^5) positions. **Table 1** shows the selection of resistor values.

The circuit uses a 74HC374 latch and MPS2222A npn transistors to interface the relays to the system CPU (**Figure 3**). The primary disadvantages of the method are board space and cost. However, for the monitor application, the circuit proved flexible and reliable. Applications that require replacing existing potentiometers or rheostats are potential candidates for this circuit. For example, you could replace a high-power rheostat with the circuit if you select relays and resistors with suitable current ratings. (DI #2167) EDN

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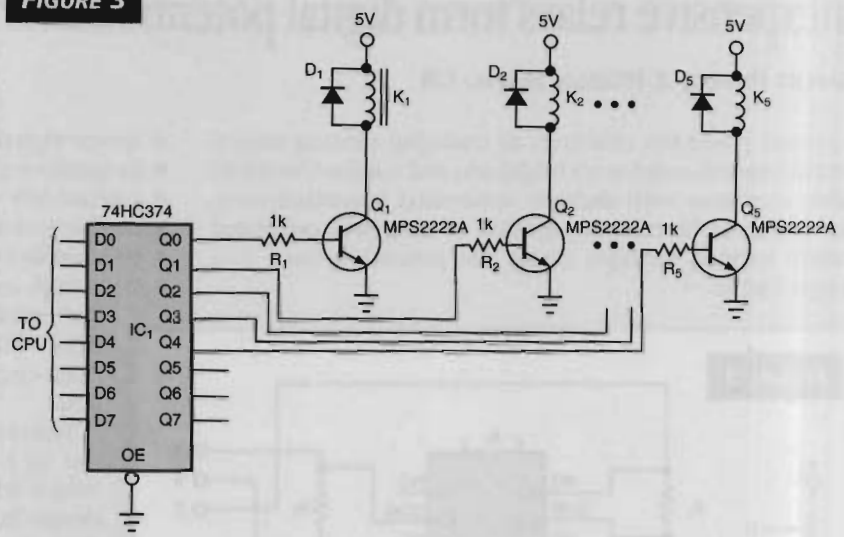
FIGURE 3



A TTL latch and a collection of inexpensive npn transistors, resistors, and relays allow you to configure a simulated potentiometer with any desired degree of resolution.

Switched-capacitor regulator provides gain

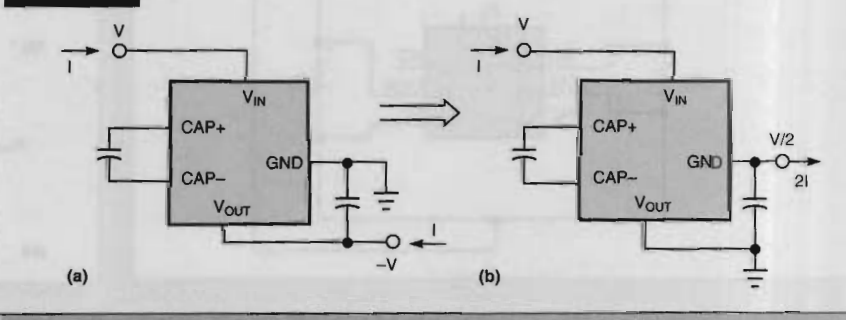
JEFF WITT, LINEAR TECHNOLOGY CORP, MILPITAS, CA

Linear voltage regulators become inefficient when the input voltage is much higher than the regulated output. The circuit in **Figure 1** dramatically increases efficiency when the input voltage is more than twice the desired output; for example, using 12V to obtain a regulated 3.3 or 5V. You usually use a switched-capacitor voltage inverter to generate a negative supply voltage from a positive input voltage. The negative-supply current is equal to the current drawn from the input. By swapping the roles of the ground and output pins, the inverter in **Figure 1** divides the input voltage by two. It also doubles the current from the input to the output, thereby providing much better efficiency than does a linear regulator.

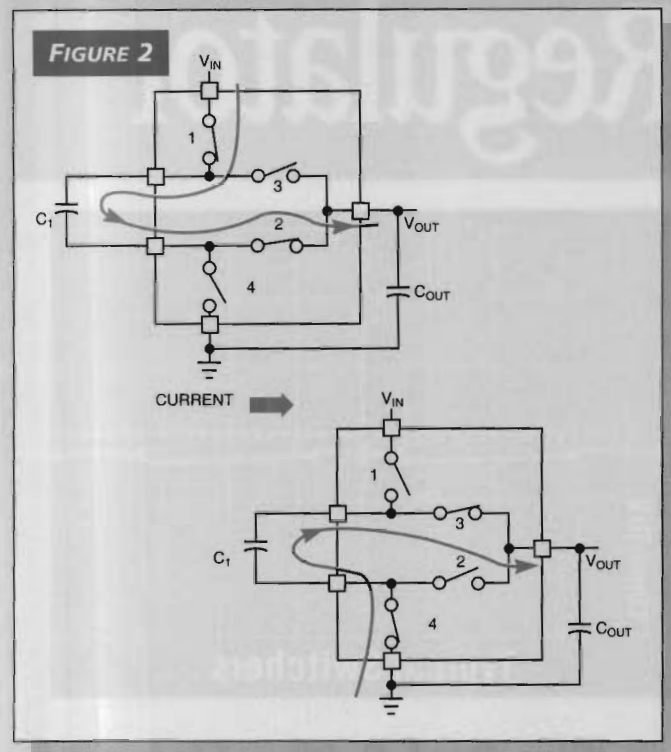
Figure 2 illustrates the circuit's operation. An internal oscillator alternately closes and opens four switches. In the first half-cycle, switches 1 and 2 close, and current flows from the input to the output, charging C_1. In the second half-cycle, switches 3 and 4 close, discharging C_1 into the output. The current delivered to the output is continuous and equal to twice the average input current. Because the current is continuous, the output-voltage ripple is low. Note that you do not need to match C_1 and C_{OUT}, because their voltages equalize on each cycle.

Figure 3 shows the actual circuit. IC_1, an LT1054 switched-capacitor voltage converter and regulator, modulates the

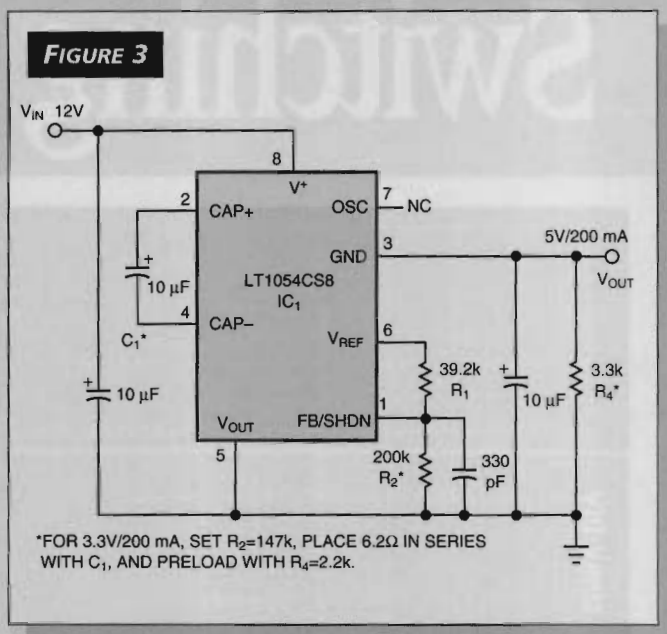
FIGURE 1



Rewiring a switched-capacitor inverter for step-down regulation results in a current gain of 2.



This switched-capacitor regulator doubles the current from the input to the output, thus increasing efficiency and eliminating the need for a heat sink.



The LT1054's internal switches alternately charge and discharge C_1, thereby delivering a continuous current to the output.

current (through switch 1 of Figure 2) to regulate the output. A servo loop keeps the potential at the FB pin equal to the potential at the GND pin. The circuit can deliver 200 mA at 5V from an input of 11.2 to 13V. Typical efficiency is 74%, compared with 42% for a linear regulator. More important, dissipation decreases from 1.4W for a linear regulator to 0.35W, a figure that IC_1's eight-pin, surface-mount package can easily handle. For a 200-mA, 3.3V output, the circuit is 49% efficient, compared with a linear regulator's 27%, with power dissipation reduced from 1.8 to 0.7W. A 6.2Ω resistor in series with C_1 shares the dissipated power with the LT1054; the circuit needs no heat sink. (DI #2168) EDN

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Precision current sink costs less than $20

CARLOS BARBERIS, BARTEK TECHNOLOGIES, HAVERHILL, MA

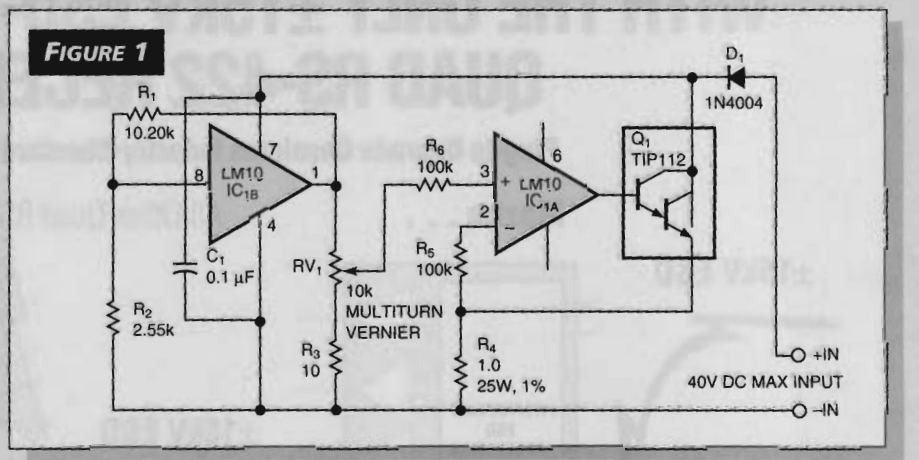
If you often need a simple active load (constant-current sink), you can benefit from the simple circuit in Figure 1. The need often arises to measure the life of a battery or other power device under constant-load conditions. The easy-to-build and inexpensive circuit in Figure 1 is a handy addition to your arsenal of test fixtures. You can build the circuit for less than $20. The most expensive parts are the vernier knob and the multiturn potentiometer. You can build the active load into a miniature enclosure with banana-jack connectors. The vernier control allows you to directly set current from 1 mA to 1A by simply dialing the desired set current. Without the vernier and multiturn potentiometer, you could build the circuit for less than $10, but you then lose the advantage of a calibrated, stand-alone test box.

The circuit is a precision current sink with typical current regulation of better than 0.5% for a 3 to 40V compliance voltage. R_4 is a sensing resistor; its voltage drop servos the input voltage to IC_{1A}. The wiper of the vernier potentiometer sets the input voltage, discounting any amplifier offset errors. The offset could be as high as 2 mV in a run-of-the-mill LM10, translating to a 2-mA error between the set current and the current flowing in R_4. The reference amplifier, IC_{1B}, is a gain-of-5 stage that provides a 1.00V reference on the high side of the current-setting potentiometer. The voltage-to-current transfer function is thus 1A/1V. You can change the transfer function to fit your needs.

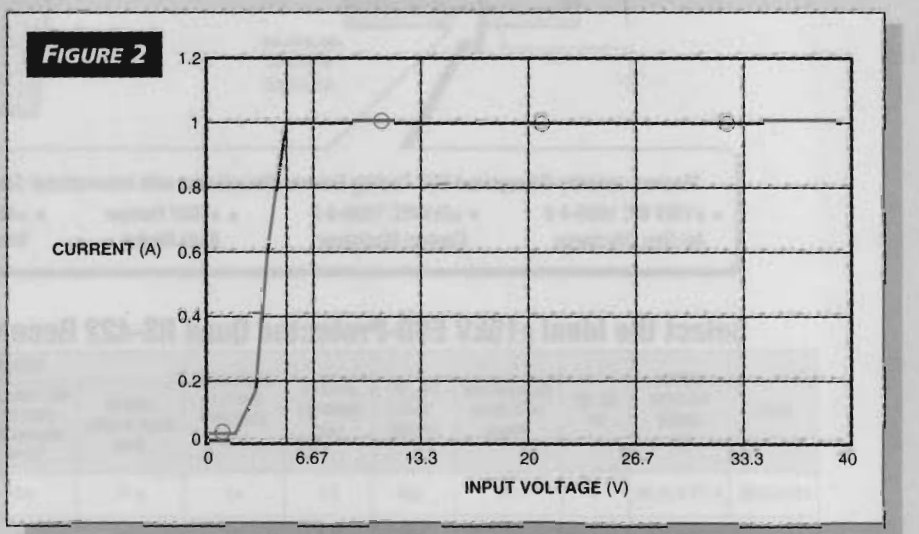
Although the current-control mechanism allows the output of the current source to approach zero, the additional currents consumed by the circuit (approximately 400 μA) establish the baseline current. Therefore, you set the bottom of the potentiometer via R_3 to start at approximately 1 mA. Under normal operation, a current setting of 1 to 300 mA maintains the setpoint within 0.5% with 3 to 40V compliance. Currents above 300 mA require 3 to 5V for compliance. The circuit maintains a 1A current within 300 μA from 4.9 to 40V or within 0.001% tolerance (**Figure 2**). You could lower the initial regulation point by one diode junction by removing D_1, whose sole purpose is to prevent destruction of the active circuitry when you connect the power supply backward.

The principal sources of error in the circuit are the amplifier offset, the tolerance of the reference voltage, the tolerance of R_4, and the fact that the current includes various branch currents other than the controlled current in the sensing resistor. These branch currents add up to approximately 400 μA, or roughly five times lower than the offset-voltage error. You can consider the error negligible for settings of 10 mA and above. The most important issue for long-term stability is efficient heat removal from the current-regulating transistor, Q_1. The transistor needs an appropriate heat sink; the choice of heat sink depends on the current ranges you need.

The element that encounters the largest voltage drop at a given current is the hottest. Q_1 dissipates V_{IN}–1W for any given input voltage when operating at 1A. If you plan to use the load on a continuous basis, for example at 1A, with a 30V input, Q_1 dissipates 29W; R_4 consumes 1W. Q_1 would thus need a hefty extruded heat sink. (DI #2171)



A handful of inexpensive parts builds a precision current sink that provides 1-mA to 1A sink current over a wide compliance-voltage range.



For compliance voltages above 4.9V, the circuit in Figure 1 provides a rock-solid 1A sink current, with less than 0.001% variation with voltage.

EDN

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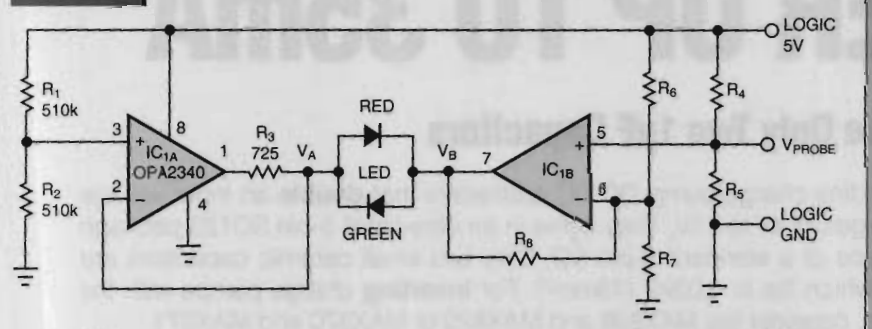
Simple logic probe uses bicolor LED

MARK SHILL, BURR-BROWN CORP, TUCSON, AZ

When probing digital logic levels on a circuit board, locating the indicator of the logic level near the probe tip is convenient, so that you can keep both the indicator and probe tip constantly in sight. When using a handheld DVM or oscilloscope probe, you must momentarily look away to read the logic level. In that instant, the probe can slip and cause a short circuit. The circuit in **Figure 1a** implements a simple handheld logic probe using just a few components. This

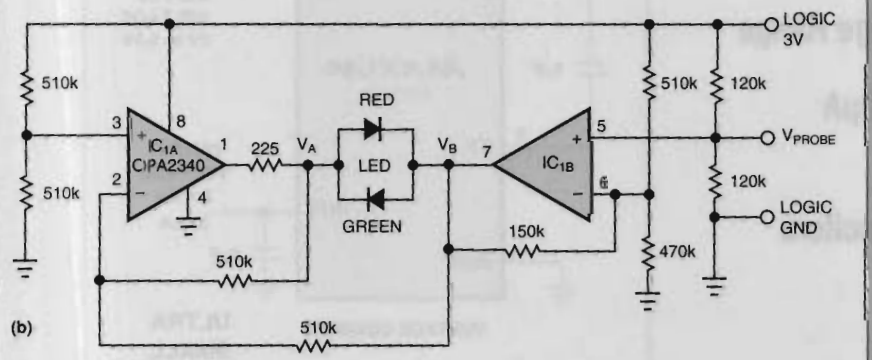
FIGURE 1



NOTE:
LED=RADIO SHACK 276-012.

RESISTOR	5V CMOS	TTL
R_4	160k	250k
R_5	120k	100k
R_6	510k	820k
R_7	270k	220k
R_8	180k	470k

(a)



(b)

A simple handheld logic probe uses a rail-to-rail op amp and a bicolor LED (a). A modified probe circuit works with 3V CMOS logic (b).

probe can measure high, low, and high-impedance logic states, in addition to indicating switching logic states. This probe is useful for quick measurements of dc logic levels. You can use a similar probe circuit (**Figure 1b**) for 3V CMOS logic.

The circuit centers around the OPA2340 dual rail-to-rail op amp and a Radio Shack 276-012 bicolor LED. The forward voltage for the red and green LEDs are 2 and 2.1V, respectively. Op amp IC_{1A} derives a buffered 2.5V reference output from the 5V supply, and R_3 limits the current to the LED when it is on. IC_{1B} buffers and amplifies the probed logic signal to a 0 to 5V output level. R_4 and R_5 set a reference level for the positive input of IC_{1B} for the case of a high-impedance level. When a logic high is present, the green LED lights; a logic low lights the red LED. When a high-impedance state is present, the LED is off.

The output voltage transfer function of IC_{1B} is

$$V_B = \left[1 + \frac{R_8(R_6 + R_7)}{R_6 \bullet R_7}\right] V_{PROBE} - \frac{R_8}{R_6} \bullet V_{CC},$$

which makes $V_{LED}=V_B-2.5V$. The values of R_6, R_7, and R_8 are such that V_B limits at the positive or negative power-supply rail when V_{PROBE} is at the logic family's minimum low or high level, respectively. **Figure 2** shows the voltage-transfer function for V_B. When V_B limits at the rail voltage, the LED lights red or green, depending on the probed logic level. When V_B is within 0.5V of the negative rail, the red LED turns on; when V_2 is within 0.4V of the positive rail, the green LED turns on. If the probe measures a high-impedance state, voltage-divider resistors R_4 and R_5 set the positive input of IC_{1B}, and the voltage across the LED is approximately 0V.

In **Figure 1b**, the output of IC_{1B} feeds in to IC_{1A}'s inverting input. For the resistor values in **Figure 1b**, the transfer function for IC_{1A} is $V_A=-V_B+3V$, thus making $V_{LED}=2V_B-3V$.
(DI #2162)

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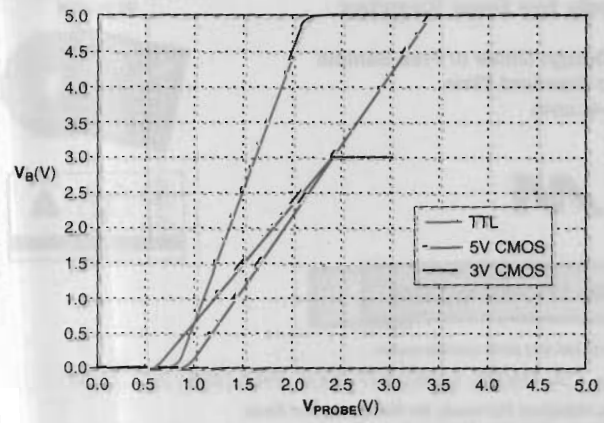
FIGURE 2



The output of IC_{1B}, V_B, limits at either the positive or negative supply rail depending on the probe voltage.

DC power wire also carries clock or data

MIKE HARDWICK, DECADE ENGINEERING, TURNER, OR

A high-side current-sense amplifier, IC_1, offers a simple method of combining low-speed clocks or other signals with dc power in cables between subsystems (**Figure 1**). Designed for monitoring charge and discharge current in secondary batteries, IC_1 outputs a current of 0.5 mA per amp of load current flowing through its internal sense resistor while rejecting common-mode supply-voltage noise. The on-chip sense resistor handles as much as 3A of continuous current. The IC accommodates power-supply voltages from 3 to 36V.

Figure 1 depicts a subsystem that receives power from its host system and simultaneously transmits a clock signal back on the same wire. The circuit uses the clock in the remote system to modulate power-supply current via an open-collector driver or discrete transistor and R_{MOD}, a switched load resistance. In the host system, IC_1 develops a voltage across R_{IV}, which represents the instantaneous sum of supply current and modulation current. R_{INTEG} and C_{INTEG} filter this voltage, biasing the comparator's reference pin to a level that tracks average power-supply current. As the signal swings above and below this reference level, the comparator outputs the recovered clock. R_{HYST} adds a small amount of hysteresis to ensure clean clock recovery.

IC_2, which comes in an SOT23-5 package, is a CMOS comparator with a rail-to-rail input range. This range allows you to choose R_{IV} with relative freedom—expect about 1V/A of load current for each 2 kΩ of resistance. The input offset of low-grade versions of IC_2, an LMC7211, can be as much as ±18 mV. Thus, select R_{MOD} and R_{IV} to produce 50 mV or more of modulation on R_{IV}, and then choose R_{HYST} to obtain a few additional millivolts of shift at this node when the comparator changes state. None of these values is critical.

For this scheme to work as expected, the power-supply current to the remote system must be relatively constant, except for the intentional modulation. Slow power-supply current variations do not cause problems, as long as you choose the integrator components with care. The integrator RC product should be about 10 times the clock period. It's convenient to choose R_{INTEG} of approximately 1 MΩ when using CMOS comparators, such as IC_2. You can then use ceramic or plastic-film capacitors for C_{INTEG}, thus minimizing the risk of failure due to capacitor leakage.

The circuit can also transmit data if the data contains little dc bias variation or if you replace the integrator components with a fixed bias source. This change means, of course, that no significant power-supply current change is allowable after calibration.

IC_1's output rise and fall times measure approximately 4 µsec, a figure similar to IC_2's response-time specification. The remote system's power-supply bypass capacitance may impose an upper bound on the clock rate because this capacitance limits the modulation rate of the supply current. This time constant is $C_{LOAD} \times (R_{SENSE}+R_{CABLE})$. R_{SENSE} is less than 0.07Ω in IC_1, and the cable's series resistance depends on the application. You must add the equivalent series resistance of the power source, connectors, and any other associated resistive elements to R_{SENSE} in this calculation if you're pushing the envelope of the circuit's performance. (DI #2175) EDN

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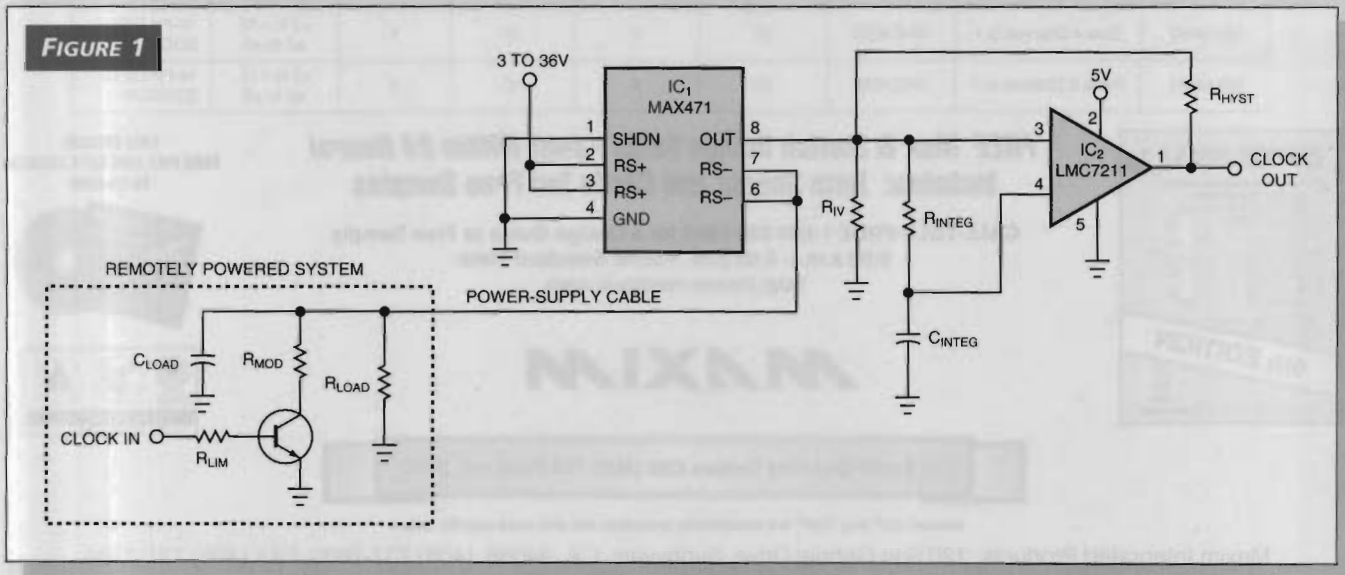
FIGURE 1



By using a high-side current-sense amplifier IC (IC_1) in an unconventional manner, you can combine clock or data signals with dc power in cables.